

SEMICONDUCTOR APPARATUS COMPRISING BIPOLAR
TRANSISTORS AND METAL OXIDE SEMICONDUCTOR
TRANSISTORS AND MANUFACTURING METHOD

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TECHNICAL FIELD OF THE INVENTION

5 [0001] The present invention is generally directed to semiconductor technology and, in particular, to a method for manufacturing a semiconductor apparatus that comprises both bipolar transistors and metal oxide semiconductor transistors.

10 **BACKGROUND OF THE INVENTION**

[0002] In recent years, there have been great advancements in the speed, power, and complexity of integrated circuits. Some integrated circuits comprise both bipolar transistors, such as PNP transistors and NPN transistors, and metal oxide
15 semiconductor (MOS) transistors, such as PMOS transistors and NMOS transistors. When integrated circuit devices are manufactured, different types of steps may be employed for manufacturing the two different types of transistors.

[0003] The process for manufacturing bipolar transistors in an
20 integrated circuit (sometimes referred to as a control flow process) involves the performance of a number of different types of steps. It is desirable that the steps for manufacturing MOS transistors on the same integrated circuit as the bipolar transistors be compatible with the steps for manufacturing the
25 bipolar transistors.

[0004] Therefore, there is a need in the art for an efficient method for combining the manufacturing steps of bipolar transistors and MOS transistors in the same integrated circuit. In particular, there is a need in the art for an improved method
5 that is capable of efficiently manufacturing bipolar transistors and MOS transistors in a unified control flow process.

SUMMARY OF THE INVENTION

[0005] To address the above-discussed deficiencies of the prior art, it is a primary object of the present invention to provide an efficient method of combining the manufacturing steps for bipolar transistors and the manufacturing steps for MOS transistors in the same integrated circuit.

[0006] The semiconductor apparatus of the present invention comprises double poly bipolar transistors and merged poly metal oxide semiconductor (MOS) transistors. The bipolar transistors and the MOS transistors are manufactured in a unified process in which a first polysilicon layer (Poly1) is doped to form the extrinsic bases in the bipolar transistors and to form the gates in the MOS transistors. The first polysilicon layer (Poly1) is patterned and etched to open a hole for the poly emitter in the bipolar transistors and to define the gate electrode in the MOS transistors. Resist material is applied and patterned and implants are performed to form the intrinsic bases of the bipolar transistors and the Lightly Doped Drains (LDD) of the MOS transistors. An advantage of this method over the prior art is that the LDDs are self aligned to the gate edge.

[0007] A dielectric layer is deposited and anisotropically etched to form spacers on the inside of the hole for the emitters of the bipolar transistors and on the outside of the gate poly for the bipolar transistors. This creates a space between the

heavily doped emitter and the heavily doped extrinsic base of the bipolar transistors and between the heavily doped sources and drains of the MOS transistors and the channel region of the MOS transistors. Persons who are skilled in the art will recognize
5 the advantage of this spacing arrangement.

[0008] A second polysilicon layer (Poly2) is doped to form emitters in the bipolar transistors and to form the sources and drains in the MOS transistors. The method of the invention minimizes the number of manufacturing process steps.

10 [0009] It is an object of the present invention to provide a method for efficiently combining the manufacturing steps for bipolar transistors and the manufacturing steps for MOS transistors in the same integrated circuit.

[0010] It is also an object of the present invention to
15 provide a method for efficiently combining the manufacturing steps for bipolar transistors and the manufacturing steps for MOS transistors in a unified process.

[0011] It is another object of the present invention to provide a method for doping a first polysilicon layer (Poly1) in
20 a semiconductor apparatus to form extrinsic bases in bipolar transistors and to form gates in MOS transistors in the semiconductor apparatus.

[0012] It is another object of the present invention to provide a method for removing the first polysilicon layer (Poly1)
25 from certain areas that are then doped to form the intrinsic

bases of the bipolar transistors and the Lightly Doped Drains (LDDs) of the MOS transistors.

[0013] It is also another object of the present invention to provide a method for self aligning the intrinsic bases to the
5 extrinsic bases and emitter of the bipolar transistors and the Lightly Doped Drains (LDDs) to the channel and source drains of the MOS transistors.

[0014] It is still another object of the present invention to provide a method for doping a second polysilicon layer (Poly2) in
10 a semiconductor apparatus to form emitters in bipolar transistors and to form sources and drains in MOS transistors in the semiconductor apparatus.

[0015] It is also an object of the present invention to provide a method for efficiently combining the manufacturing
15 steps for bipolar transistors and the manufacturing steps for MOS transistors in the same integrated circuit that minimizes the number of manufacturing process steps.

[0016] The foregoing has outlined rather broadly the features and technical advantages of the present invention so that those
20 persons who are skilled in the art may better understand the detailed description of the invention that follows. Additional features and advantages of the invention will be described hereinafter that form the subject of the claims of the invention. Persons who are skilled in the art should appreciate that they
25 may readily use the conception and the specific embodiment

disclosed as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. Persons who are skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope
5 of the invention in its broadest form.

[0017] Before undertaking the Detailed Description of the Invention below, it may be advantageous to set forth definitions of certain words and phrases used throughout this patent document: the terms "include" and "comprise," as well as
10 derivatives thereof, mean inclusion without limitation; the term "or," is inclusive, meaning and/or; the phrases "associated with" and "associated therewith," as well as derivatives thereof, may mean to include, be included within, interconnect with, contain, be contained within, connect to or with, couple to or with, be
15 communicable with, cooperate with, interleave, juxtapose, be proximate to, be bound to or with, have, have a property of, or the like; and the term "controller" means any device, system or part thereof that controls at least one operation, such a device may be implemented in hardware, firmware or software, or some
20 combination of at least two of the same. It should be noted that the functionality associated with any particular controller may be centralized or distributed, whether locally or remotely. Definitions for certain words and phrases are provided throughout this patent document, those persons of ordinary skill in the art
25 should understand that in many, if not most instances, such

definitions apply to prior uses, as well as future uses, of such defined words and phrases.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] For a more complete understanding of the present invention and its advantages, reference is now made to the following description taken in conjunction with the accompanying
5 drawings, in which like reference numerals represent like parts:

[0019] FIGURE 1 illustrates a substrate comprising an active silicon layer on a buried oxide layer on a handle wafer for use in manufacturing a semiconductor device according to the principles of the present invention;

10 [0020] FIGURE 2 illustrates four portions of the substrate shown in FIGURE 1 in which an NPN semiconductor device, and a PNP semiconductor device, and an NMOS semiconductor device, and a PMOS semiconductor device will be manufactured in accordance with the principles of the present invention. FIGURE 2 also
15 illustrates an implant procedure for forming an NPN buried layer (NBL) in the NPN device and in the PMOS device;

[0021] FIGURE 3 illustrates the location of the NPN buried layer (NBL) in the NPN device and in the PMOS device;

[0022] FIGURE 4 illustrates an implant procedure for forming
20 an PNP buried layer (PBL) in the PNP device and in the NMOS device;

[0023] FIGURE 5 illustrates the location of the PNP buried layer (PBL) in the PNP device and in the NMOS device and an N-epi layer grown over all four semiconductor devices;

[0024] FIGURE 6 illustrates the location of a layer of Epi oxide grown over all four semiconductor devices;

[0025] FIGURE 7 illustrates an implant procedure for forming a P well in the PNP device;

5 [0026] FIGURE 8 illustrates the location of the P well in the PNP device and an implant procedure for forming an N+ sinker in the NPN device and in the PMOS device;

[0027] FIGURE 9 illustrates the location of the N+ sinker in the NPN device and in the PMOS device and an implant procedure
10 for forming an P+ sinker in the PNP device and in the NMOS device;

[0028] FIGURE 10 illustrates the location of the P+ sinker in the PNP device and in the NMOS device and the deposition of a nitride layer over the layer of Epi oxide on all four
15 semiconductor devices;

[0029] FIGURE 11 illustrates the result of performing a shallow trench mask etch on each of the four semiconductor devices;

[0030] FIGURE 12 illustrates the result of performing an
20 implantation procedure for forming channel stops in the shallow trench areas of the PNP device and of the NMOS device. The NPN device and the PMOS device are covered with a mask layer;

[0031] FIGURE 13 illustrates the result of a mask and etch procedure for forming deep trenches to isolate each of the four
25 semiconductor devices;

[0032] FIGURE 14 illustrates the deposition of a trench liner oxidation layer on the four semiconductor devices;

[0033] FIGURE 15 illustrates the deposition of a trench fill oxide base layer over the four semiconductor devices;

5 [0034] FIGURE 16 illustrates the result of performing an etch back of the trench fill oxide base layer over the four semiconductor devices;

[0035] FIGURE 17 illustrates the application of a trench fill oxidation layer over the four semiconductor devices;

10 [0036] FIGURE 18 illustrates the application of a reverse trench mask and a partial wet etch procedure over the four semiconductor devices;

[0037] FIGURE 19 illustrates the application of a chemical mechanical polishing (CMP) procedure over the four semiconductor
15 devices;

[0038] FIGURE 20 illustrates the application of a nitride and oxide wet strip procedure over the four semiconductor devices;

[0039] FIGURE 21 illustrates the application of a sacrificial oxide layer over the four semiconductor devices;

20 [0040] FIGURE 22 illustrates the application of a procedure for implanting a CMOS N Well in the PMOS device;

[0041] FIGURE 23 illustrates the application of a procedure for implanting a CMOS P Well in the NMOS device;

[0042] FIGURE 24 illustrates the application of a pre-gate plasma etch procedure and the growth of a gate oxide layer over the four semiconductor devices;

[0043] FIGURE 25 illustrates the deposition of a protective
5 layer of polysilicon over the four semiconductor devices;

[0044] FIGURE 26 illustrates the application of a procedure for etching the protective polysilicon layer from the NPN device and from the PNP device. The protective polysilicon layer on the NMOS device and on the PMOS device is covered with a mask layer;

10 [0045] FIGURE 27 illustrates the deposition of a first layer of polysilicon (Poly1) over the four semiconductor devices;

[0046] FIGURE 28 illustrates an implantation procedure for doping a portion of the Poly1 layer of the PNP device to form an extrinsic base in the PNP device and a portion of the Poly1 layer
15 of the NMOS device to form an NMOS gate. The NPN device and the PMOS device are covered with a mask layer;

[0047] FIGURE 29 illustrates an implantation procedure for doping a portion of the Poly1 layer of the NPN device to form an extrinsic base in the NPN device and a portion of the Poly1 layer
20 of the PMOS device to form a PMOS gate. The PNP device and the NMOS device are covered with a mask layer;

[0048] FIGURE 30 illustrates the deposition of a layer of an Inter Poly Dielectric (IPD) over the four semiconductor devices;

[0049] FIGURE 31 illustrates the result of performing a mask
25 and etch procedure to etch portions of the Inter Poly Dielectric

(IPD) layer and portions of the Poly1 layer over the NPN device and over the PNP device. The NMOS device and the PMOS device are covered with a mask layer;

[0050] FIGURE 32 illustrates the result of performing a mask
5 and etch procedure to etch portions of the Inter Poly Dielectric (IPD) layer and portions of the Poly1 layer over the NMOS device and over the PMOS device. The NPN device and the PNP device that were previously etched are covered with a mask layer;

[0051] FIGURE 33 illustrates the result of a diffusion and
10 oxidation procedure in which dopant from the extrinsic base diffuses into the diffused extrinsic base areas of the NPN device and the PNP device;

[0052] FIGURE 34 illustrates an implantation procedure for
doping an intrinsic base of the NPN device and for doping a
15 Lightly Doped Drain (LDD) of the PMOS device. The PNP device and the NMOS device are covered with a mask layer;

[0053] FIGURE 35 illustrates an implantation procedure for
doping an intrinsic base of the PNP device and for doping a
Lightly Doped Drain (LDD) of the NMOS device. The NPN device and
20 the PMOS device that were previously doped are covered with a mask layer;

[0054] FIGURE 36 illustrates the deposition of a nitride spacer layer over the four semiconductor devices;

[0055] FIGURE 37 illustrates the result of an etch back
25 procedure applied to the nitride spacer layer;

[0056] FIGURE 38 illustrates the deposition of a second layer of polysilicon (Poly2) over the four semiconductor devices;

[0057] FIGURE 39 illustrates an implantation procedure for doping a portion of the Poly2 layer to form an emitter and a deep collector of the NPN device and for doping a portion of the Poly2 layer to form an NMOS source/drain in the NMOS device and for doping a portion of the Poly2 layer to form a well contact of the PMOS device. The PNP device is covered with a mask layer;

[0058] FIGURE 40 illustrates an implantation procedure for doping a portion of the Poly2 layer to form an emitter and a deep collector of the PNP device and for doping a portion of the Poly2 layer to form a well contact of the NMOS device and for doping a portion of the Poly2 layer to form a PMOS source/drain of the PMOS device. The NPN device that was previously doped is covered with a mask layer;

[0059] FIGURE 41 illustrates the result of performing a mask and etch procedure to etch portions of the Poly2 layer to define the emitters and collectors of the NPN device and of the PNP device and to define the sources and drains of the NMOS device and of the PMOS device;

[0060] FIGURE 42 illustrates the result of performing an etch procedure to etch portions of the Inter Poly Dielectric (IPD) layer and portions of the trench fill material on each of the four semiconductor devices;

[0061] FIGURE 43 illustrates the result of applying a Rapid Thermal Process (RTP) to activate the emitters in the NPN device and in the PNP device and to active the sources and drains in the NMOS device and in the PMOS device;

5 [0062] FIGURE 44 illustrates a diagrammatic plan view of the top of an exemplary rectangular opening etched into a doped Poly1 layer of a bipolar semiconductor device of the invention;

[0063] FIGURE 45 illustrates the formation of a layer of cobalt silicide to cover all Poly2 layers and all Poly1 layers
10 that are not under a Poly2 layer;

[0064] FIGURE 46 illustrates the deposition of a layer of tetra ethyl ortho silicate (TEOS) over the four semiconductor devices;

[0065] FIGURE 47 illustrates the result of performing a mask
15 and etch procedure to etch portions of the layer of tetra ethyl ortho silicate (TEOS) over the four semiconductor devices to receive metal contacts;

[0066] FIGURE 48 illustrates the placement of metal contacts within contact receptacles in the four semiconductor devices;

20 [0067] FIGURE 49 illustrates a diagrammatic top plan view of the layout of an exemplary bipolar transistor of the invention;
and

[0068] FIGURE 50 illustrates a diagrammatic top plan view of the layout of an exemplary metal oxide semiconductor (MOS)
25 transistor of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0069] FIGURES 1 through 50, discussed below, and the various embodiments used to describe the principles of the present invention in this patent document are by way of illustration only and should not be construed in any way to limit the scope of the invention. Persons who are skilled in the art will understand that the principles of the present invention may be implemented in any type of suitably arranged semiconductor device.

[0070] FIGURE 1 illustrates a substrate 100 for use in manufacturing a semiconductor device according to the principles of the present invention. The foundation of substrate 100 comprises a handle wafer 110 on which a buried oxide layer 120 is formed. An active silicon layer 130 is formed on the buried oxide layer 120. In an advantageous embodiment of the invention the thickness of the active silicon layer 130 is approximately two and two tenths microns ($2.2\ \mu$) and the thickness of the buried oxide layer 120 is approximately one micron ($1.0\ \mu$). The buried oxide layer 120 insulates the handle wafer 110 from the active silicon layer 130 to eliminate leakage and reduce capacitance. The handle wafer 110 will be shown only in FIGURE 1.

[0071] Persons who are skilled in the art will recognize that substrate 100 shown in FIGURE 1 is part of a silicon on insulator (SOI) isolation architecture. The semiconductor devices that will be more fully described in this patent document can also be isolated by other types of isolation architectures such as

(1) junction isolation, (2) deep and/or shallow trenches filled with oxide and/or polysilicon, and (3) local oxidation of silicon. This list of alternative isolation architectures is not exhaustive and other types of isolation architectures may also be
5 used.

[0072] A layer of screen oxide 140 is then applied to the surface of the active silicon layer 130. In an advantageous embodiment of the invention the thickness of the screen oxide 140 is approximately two hundred fifty Ångstroms (250 Å) or twenty
10 five thousandths of a micron (0.025 μ).

[0073] FIGURE 2 illustrates four portions of the substrate shown in FIGURE 1. The steps of the manufacturing method of the present invention will be described for an NPN bipolar transistor semiconductor device, and a PNP bipolar transistor semiconductor
15 device, and an NMOS transistor semiconductor device, and a PMOS transistor semiconductor device. Although the four semiconductor devices are shown separately in FIGURE 2, the four semiconductor devices are all located on and manufactured from the same substrate 100.

[0074] FIGURE 2 illustrates an implant procedure for forming an NPN buried layer (NBL) 220 in the NPN device and an NPN buried layer (NBL) 230 in the PMOS device. A photoresist mask 210 is placed over the four devices and openings are etched through the photoresist mask 210 over the NPN device and the PMOS device. The
25 arrows in FIGURE 2 illustrate the implant doping procedure for

forming the NPN buried layers. FIGURE 3 illustrates the location of NPN buried layer (NBL) 220 in the NPN device and the location of NPN buried layer (NBL) 230 in the PMOS device.

[0075] FIGURE 4 illustrates an implant procedure for forming a PNP buried layer (PBL) 420 in the PNP device and a PNP buried layer (PBL) 430 in the NMOS device. A photoresist mask 410 is placed over the four devices and openings are etched through the photoresist mask 410 over the PNP device and over the NMOS device. The arrows in FIGURE 4 illustrate the implant doping procedure for forming the PNP buried layers. FIGURE 5 illustrates the location of PNP buried layer (PBL) 420 in the PNP device and the location of PNP buried layer (PBL) 430 in the NMOS device.

[0076] An N-epitaxial layer (N-epi) 510 is then grown over the four semiconductor devices (NPN, PNP, NMOS, PMOS). In an advantageous embodiment of the invention the thickness of the N-epi layer 510 is approximately two and one tenth microns (2.1μ). FIGURE 5 illustrates the placement of the N-epi layer 510 over the four semiconductor devices.

[0077] Persons who are skilled in the art will recognize that a P-epitaxial layer (P-epi) (not shown) or an undoped epitaxial layer (not shown) could also be used as long as an appropriate doping was executed. Specifically, with a P-epi the PNP device would not need a P well, but the NPN device would need an N well. With an intrinsic epi both the PNP device and the NPN device would need an appropriate well. Alternatively, the NPN and PNP

devices could be formed without epi, either by using a high energy implant process to form the buried layers or by forming the devices without buried layers.

[0078] A layer of epi oxide 610 is then applied to the surface of the N-epi layer 510 as shown in FIGURE 6. In an advantageous embodiment of the invention the thickness of the epi oxide 610 is approximately two hundred fifty Ångstroms (250 Å) or twenty five thousandths of a micron (0.025 μ). To simplify the drawings the reference numerals from previous drawings will generally not be repeated for structures that have already been identified.

[0079] In the next step of the manufacturing method of the invention a P well is formed in the PNP device. FIGURE 7 illustrates an implant procedure for forming a P well in the PNP device. A photoresist mask 710 is placed over the four devices and openings are etched through the photoresist mask 710 over the PNP device. The arrows in FIGURE 7 illustrate the implant doping procedure for forming the P well 720. FIGURE 7 and FIGURE 8 illustrate the location of the P well 720 in the PNP device.

[0080] In the next step of the manufacturing method of the invention an N+ sinker is formed in the NPN device and an N+ well contact is formed in the PMOS device. FIGURE 8 illustrates an implant procedure for forming an N+ sinker 820 in the NPN device and an N+ well contact 830 in the PMOS device. A photoresist mask 810 is placed over the four devices and openings are etched through the photoresist mask 810 over the NPN device and over the

PMOS device. The arrows in FIGURE 8 illustrate the implant doping procedure for forming the N+ sinker 820 and the N+ well contact 830. FIGURE 8 and FIGURE 9 illustrate the location of N+ sinker 820 in the NPN device and the location of N+ well contact 830 in the PMOS device.

[0081] In the next step of the manufacturing method of the invention a P+ sinker is formed in the PNP device and a P+ well contact is formed in the NMOS device. FIGURE 9 illustrates an implant procedure for forming a P+ sinker 920 in the PNP device and a P+ well contact 930 in the NMOS device. A photoresist mask 910 is placed over the four devices and openings are etched through the photoresist mask 910 over the PNP device and over the NMOS device. The arrows in FIGURE 9 illustrate the implant doping procedure for forming the P+ sinker 920 and the P+ well contact 930. FIGURE 9 and FIGURE 10 illustrate the location of P+ sinker 920 in the PNP device and the location of P+ well contact 930 in the NMOS device.

[0082] Persons who are skilled in the art will recognize that the sinkers and buried layers described above are not essential to either the bipolar transistor devices or the MOS transistor devices. The sinkers and buried layers described above represent a best mode of the apparatus of the present invention.

[0083] In the next step of the manufacturing method of the invention the photoresist mask is removed and a layer of nitride 1010 is deposited on the surfaces of the four devices. In an

advantageous embodiment of the invention the thickness of the nitride layer 1010 is approximately one thousand eight hundred fifty Ångstroms (1850 Å) or one hundred eighty five thousandths of a micron (0.185 μ). FIGURE 10 illustrates the location of the
5 nitride layer 1010.

[0084] In the next step of the manufacturing method of the invention a shallow trench mask and etch procedure is performed. FIGURE 11 illustrates the result of performing the shallow trench mask and etch procedure on each of the four semiconductor
10 devices. As shown in FIGURE 11, a photoresist mask 1110 is placed over the four devices and openings are etched through the photoresist mask 1110 over the devices. The arrows in FIGURE 11 represent the etch procedure. In an advantageous embodiment of the invention the etch procedure etches through the 0.185 micron
15 thick nitride layer 1010, then through the 0.025 micron thick epi oxide layer 610, and then through a thickness of approximately one and thirty four hundredths micron (1.34 μ) of the underlying active silicon layer 130.

[0085] Persons who are skilled in the art will recognize that
20 the shallow trench isolation technique is one of several methods that are available for separating individual components within a transistor or for separating individual devices from each other. The shallow trench isolation technique represents a best mode of the apparatus of the invention. As previously mentioned, other
25 types of isolation techniques may also be used.

[0086] In the next step of the manufacturing method of the invention a mask and implant procedure is performed to form channel stops in the PNP device and in the NMOS device. FIGURE 12 illustrates the procedure. The previous photoresist mask 1110 is removed and the four semiconductor devices are covered with a photoresist mask 1210. The photoresist mask 1210 then etched to create openings over the PNP device and over the NMOS device. The arrows in FIGURE 12 illustrate the implant doping procedure for forming the channel stops. Channel stops 1220, 1230 and 1240 are formed in the shallow trench areas of the PNP device. Channel stops 1250, 1260 and 1270 are formed in the shallow trench areas of the NMOS device.

[0087] Persons who are skilled in the art will recognize that the channel stops may or may not be necessary depending upon the details of the isolation technique that is used.

[0088] In the next step of the manufacturing method of the invention a mask and etch procedure is performed to form deep trenches to isolate the NPN device, the PNP device, the NMOS device, and the PMOS device, respectively. As shown in FIGURE 13, a photoresist mask 1310 is applied over the four devices. The photoresist mask 1310 is then etched to create openings at the edges of each of the four devices. The arrows in FIGURE 13 illustrate the etch procedure for forming the deep trenches 1320. In an advantageous embodiment of the invention each deep trench 1320 is approximately three and five tenths microns (3.5μ)

microns to four and seven tenths microns (4.7μ) in depth and approximately one micron (1.0μ) in width. Each deep trench 1320 extends to and contacts the underlying buried oxide layer 120.

[0089] Persons who are skilled in the art will recognize that
5 the deep trench isolation technique is one of several methods that are available for separating individual devices from each other. The deep trench isolation technique represents a best mode of the apparatus of the invention. As previously mentioned, other types of isolation techniques may also be used.

10 [0090] In the next step of the manufacturing method of the invention a trench liner oxidation layer is placed over each of the four devices. FIGURE 14 illustrates the location of the trench liner oxidation layer 1410. In an advantageous embodiment of the invention the trench liner oxidation layer 1410 is
15 approximately six hundred fifty Ångstroms (650 Å) or sixty five thousandths of a micron (0.065μ).

[0091] The trench liner oxidation layer step also serves to anneal the implant damage from the preceding implants. The trench liner oxidation layer step also diffuses the sinkers and well
20 through the epi to the buried layers.

[0092] In the next step of the manufacturing method of the invention a trench fill oxide base layer is placed over the four devices. FIGURE 15 illustrates the location of the trench fill oxide base layer 1510. In an advantageous embodiment of
25 the invention the trench fill oxide base layer 1510 is

approximately three thousand Ångstroms (3000 Å) or three tenths of a micron (0.30 μ).

[0093] The use of trench fill oxide base layer 1510 represents a best mode of the apparatus of the invention. The trench fill
5 material that is used could be another type of dielectric material, or a polysilicon material, or some other suitable material. Alternatively, the trench could be oxidized closed.

[0094] In the next step of the manufacturing method of the invention the trench fill oxide base layer 1510 is etched back.
10 FIGURE 16 illustrates the etched form of the trench fill oxide base layer 1510. In an advantageous embodiment of the invention the trench fill oxide base layer 1510 is etched back so that its thickness is approximately two thousand four hundred Ångstroms (2400 Å) or twenty four hundredths of a micron (0.240 μ).

15 [0095] The etch back step for the trench fill is necessary only if the aspect ratio of the trench is such that an improvement is needed to close the gap between the sidewalls of the trench as the trench fill material is deposited.

[0096] An oxide layer 1710 is placed over the NPN device, the
20 PNP device, the NMOS device, and the PMOS device, respectively. In an advantageous embodiment of the invention the thickness of the oxide layer 1710 is approximately sixteen thousand six hundred Ångstroms (16,600 Å) or one and sixty six hundredths micron (1.66 μ). The placement of oxide layer 1710 is illustrated
25 in FIGURE 17.

[0097] In the next step of the manufacturing method of the invention a reverse trench mask and a partial wet etch procedure are performed. A photoresist mask 1820 is then placed over the oxide layer 1710. The placement of photoresist mask 1820 is
5 illustrated in FIGURE 18. The photoresist mask 1820 then etched to create openings over the active areas of the four semiconductor devices. A partial wet etch is then performed to etch the oxide layer 1710 over the active areas. In an advantageous embodiment of the invention the wet etch procedure
10 leaves a thickness of oxide layer 1710 over the active areas that is equal to approximately three thousand Ångstroms (3000 Å) or three tenths of a micron (0.30 μ).

[0098] The reverse trench mask and the partial wet etch procedure shown in FIGURE 18 is an optional step. The reverse
15 trench mask and the partial wet etch simplifies the chemical mechanical polishing (CMP) procedure. The simplification of the CMP could be addressed in other ways (such as pattern density rules) or omitted altogether.

[0099] In the next step of the manufacturing method of the invention the photoresist mask 1820 is removed and a chemical
20 mechanical polishing (CMP) procedure is applied to the four semiconductor devices. FIGURE 19 illustrates the result of applying the chemical mechanical polishing (CMP) procedure. In an advantageous embodiment of the invention the thickness of
25 the nitride layer 1010 is approximately nine hundred fifty

Ångstroms (950 Å) or ninety five thousandths of a micron (0.095 μ).

[00100] In the next step of the manufacturing method of the invention a trench fill densification procedure is performed.

5 The trench fill densification procedure densifies the deposited dielectric oxide layer 1710. The trench fill densification procedure also serves to complete diffusion of the sinkers and bipolar P well.

[00101] In the next step of the manufacturing method of the invention a nitride and oxide wet strip procedure is performed on
10 the four semiconductor devices. First the oxide layer 1710 is etched down to the surface of the nitride layer 1010 in each device. Then the nitride layer 1010 in each device is stripped away. Then the oxide layer 610 located under the nitride layer
15 1010 is also stripped away. FIGURE 20 illustrates the appearance of the NPN device, the PNP device, the NMOS device and the PMOS device after these steps have been taken.

[00102] In the next step of the manufacturing method of the invention a sacrificial oxide layer is applied over the active
20 areas of the four semiconductor devices. FIGURE 21 illustrates the location of the sacrificial oxide layer 2110. In an advantageous embodiment of the invention the thickness of the sacrificial oxide layer 2110 is approximately four hundred Ångstroms (400 Å) or four hundredths of a micron (0.04 μ).

[00103] In the next step of the manufacturing method of the invention a CMOS N well is implanted in the PMOS device. FIGURE 22 illustrates the application of the procedure for implanting a CMOS N Well 2220 in the PMOS device. A photoresist mask 2210 is placed over the four devices and an opening is etched through the photoresist mask 2210 over the PMOS device. The arrows in FIGURE 22 illustrate the implant doping procedure for forming the CMOS N well 2220 in the PMOS device.

[00104] In the next step of the manufacturing method of the invention a CMOS P well is implanted in the NMOS device. FIGURE 23 illustrates the application of the procedure for implanting a CMOS P Well 2320 in the NMOS device. The photoresist mask 2210 is removed and a photoresist mask 2310 is placed over the four devices. An opening is etched through the photoresist mask 2310 over the NMOS device. The arrows in FIGURE 23 illustrate the implant doping procedure for forming the CMOS P well 2320 in the NMOS device.

[00105] This advantageous embodiment of the invention uses implanted retrograde wells with included threshold adjust and anti-punchthrough implants through a sacrificial oxide. This embodiment represents the best mode of the apparatus of the invention. Persons who are skilled in the art will recognize that other methods exist for forming the well and channel doping including (but not limited to) an earlier implanted and driven well (with or without threshold adjust) either through a

sacrificial oxide through the gate oxide or through the gate poly and gate oxide.

[00106] In the next step of the manufacturing method of the invention the photoresist mask 2310 is removed. A pre-gate
5 plasma etch procedure is then performed. Then the oxide layer 1710 is etched down to the level of the surface of the CMOS P well 2320 and the surface of the CMOS N well 2220. The oxide layer 1710 is also etched down to the level of the surface of the NPN device and the PNP device. Then a gate oxide layer 2410 is
10 grown over the active areas of the four semiconductor devices. FIGURE 24 illustrates the result. In an advantageous embodiment of the invention the thickness of the gate oxide layer 2410 is approximately one hundred fifty Ångstroms (150 Å) or fifteen thousandths of a micron (0.015 μ).

15 [00107] The pre-gate plasma etch procedure is not part of the invention. The pre-gate plasma etch procedure is an optional step that is used to improve gate oxide integrity. Other control flow processes may use a shallow trench technique without using the pre-gate plasma etch procedure.

20 [00108] In the next step of the manufacturing method of the invention a protective layer of polysilicon is deposited over the four semiconductor devices. FIGURE 25 shows the protective layer of polysilicon 2510. The purpose of the protective layer of polysilicon 2510 is to protect the NMOS device and the PMOS
25 device. In an advantageous embodiment of the invention the

thickness of the polysilicon layer 2510 is approximately one thousand Ångstroms (1000 Å) or one tenth of a micron (0.10 μ).

[00109] In the next step of the manufacturing method of the invention the polysilicon layer 2510 is removed from the NPN device and from the PNP device. A photoresist mask 2610 is placed over the NMOS device and over the PMOS device. The polysilicon layer 2510 is then etched from the NPN device and from the PNP device. As shown in FIGURE 26, the polysilicon layer 2510 remains in place over the NMOS device and over the PMOS device.

[00110] Persons who are skilled in the art will recognize this step as a merged poly method that is commonly used in Bipolar CMOS (BiCMOS) devices with poly emitters. The merged poly method represents a best mode of the apparatus of the invention. Alternatively, this process could be done without the merged poly and masking and etching the gate oxide prior to the deposition of the first layer of polysilicon (Poly1).

[00111] In the next step of the manufacturing method of the invention the photoresist mask 2610 is removed from the NMOS device and from the PMOS device. A selective etch is performed that removes the gate oxide 2410 from the NPN device and the PNP device but does not etch the poly protect layer 2510 or the underlying gate oxide 2410 on the PMOS device or the NMOS device.

A layer of polysilicon 2700 (Poly1) is then deposited on the four semiconductor devices. FIGURE 27 illustrates the deposition of the layer of polysilicon 2700 (Poly1) over the four semiconductor

devices. The layer of polysilicon 2700 covers the protective layer of polysilicon 2510 on the NMOS device and on the PMOS device. The layer of polysilicon 2700 is in direct contact with the monosilicon in the NPN device and the PNP device. In an
5 advantageous embodiment of the invention the thickness of the layer of polysilicon 2700 (Poly1) is approximately two thousand Ångstroms (2000 Å) or two tenths of a micron (0.20 μ).

[00112] In the next step of the manufacturing method of the invention a portion of the Poly1 layer (polysilicon layer 2700)
10 is doped to form an extrinsic base in the PNP device and an NMOS gate in the NMOS device. FIGURE 28 illustrates the implantation procedure. A photoresist mask 2800 is placed over the four semiconductor devices and openings are etched through the photoresist mask 2800 over the PNP device and over the NMOS
15 device. The three arrows in FIGURE 28 illustrate the implant doping procedure for doping the polysilicon layer 2700 to form an extrinsic base in the PNP device. The doped portion is denoted with the reference numeral 2810. The single arrow in FIGURE 28 illustrates the implant doping procedure for doping the
20 polysilicon layer 2700 (and the polysilicon layer 2510) to form an NMOS gate in the NMOS device. The doped portion is denoted with the reference numeral 2820.

[00113] Persons who are skilled in the art will recognize that the method described above is one of several available methods
25 for doping the polysilicon layer 2700 (and the polysilicon layer

2510). Some of the other available methods include (1) diffusion from a doped glass and (2) in situ doping of the polysilicon with phosphorus or arsenic.

[00114] In the next step of the manufacturing method of the invention a portion of the Poly1 layer (polysilicon layer 2700) is doped to form an extrinsic base in the NPN device and a PMOS gate in the PMOS device. FIGURE 29 illustrates the implantation procedure. A photoresist mask 2900 is placed over the four semiconductor devices and openings are etched through the photoresist mask 2900 over the NPN device and over the PMOS device. The three arrows in FIGURE 29 illustrate the implant doping procedure for doping the polysilicon layer 2700 to form an extrinsic base in the NPN device. The doped portion is denoted with the reference numeral 2910. The single arrow in FIGURE 29 illustrates the implant doping procedure for doping the polysilicon layer 2700 (and the polysilicon layer 2510) to form a PMOS gate in the PMOS device. The doped portion is denoted with the reference numeral 2920.

[00115] As previously mentioned, persons who are skilled in the art will recognize that the method described above is one of several available methods for doping the polysilicon layer 2700. Other methods also exist for doping the polysilicon layer 2700.

[00116] In the next step of the manufacturing method of the invention a layer of an Inter Poly Dielectric (IPD) is deposited over the four semiconductor devices. FIGURE 30 illustrates the

result of the deposition of the Inter Poly Dielectric (IPD) layer 3000. The Inter Poly Dielectric (IPD) layer 3000 is made up of undoped TEOS. In an advantageous embodiment of the invention the thickness of the Inter Poly Dielectric (IPD) layer 3000 is approximately two thousand three hundred Ångstroms (2300 Å) or
5 twenty three hundredths of a micron (0.23μ).

[00117] Persons who are skilled in the art will recognize that alternative types of dielectrics may also be used. For example, silicon nitride may be used in place of undoped TEOS in Inter
10 Poly Dielectric (IPD) layer 3000. Alternative methods also exist for forming the Inter Poly Dielectric (IPD) layer 3000. For example, the IPD layer 3000 may be formed with a spin on glass (SOG) method, by a chemical vapor deposition (CVD) method, or by oxidizing part of the poly layer itself.

15 [00118] In the next step of the manufacturing method of the invention a mask and etch procedure is performed to etch portions of the Inter Poly Dielectric (IPD) layer 3000 and portions of the Poly1 layer 2700 over the NPN device and over the PNP device. FIGURE 31 illustrates the mask and etch procedure. A photoresist
20 mask 3100 is placed over the four semiconductor devices. Openings are etched through the photoresist mask 3100 over the NPN device and over the PNP device. The photoresist mask 3100 covers the NMOS device and the PMOS device.

[00119] As shown in FIGURE 31, the etch procedure etches
25 through the Inter Poly Dielectric (IPD) layer 3000 located over

the doped Poly1 layer 2910 to form extrinsic bases in the NPN device. The etch procedure then etches through the doped Poly1 layer 2910 to form a passageway through the doped Poly1 layer 2910 down to the underlying E epi layer 510. In one advantageous embodiment the boundaries of the passageway are in the form of a rectangle. In the cross sectional view shown in FIGURE 31 the passageway apparently divides doped Poly1 layer 2910 into a first portion 3120 and a second portion 3130. The portion of the doped Poly1 layer 2910 that is represented by the first portion 3120 and the portion of the doped Poly1 layer 2910 that is represented by the second portion 3130 are actually connected by unetched portions of doped Poly1 layer 2910 (not shown in FIGURE 31). Similarly, the etch procedure also etches through the Inter Poly Dielectric (IPD) layer 3000 and the undoped Poly1 layer 2700 down to the N+ sinker 820 in the NPN device.

[00120] As also shown in FIGURE 31, the etch procedure etches through the Inter Poly Dielectric (IPD) layer 3000 located over the doped Poly1 layer 2810 to form extrinsic bases in the PNP device. The etch procedure then etches through the doped Poly1 layer 2810 to form a passageway through the doped Poly1 layer 2810 down to the underlying P well 720. In one advantageous embodiment the boundaries of the passageway are in the form of a rectangle. In the cross sectional view shown in FIGURE 31 the passageway apparently divides doped Poly1 layer 2810 into a first portion 3140 and a second portion 3150. The portion of the doped

Poly1 layer 2810 that is represented by the first portion 3140 and the portion of the doped Poly1 layer 2810 that is represented by the second portion 3150 are actually connected by unetched portions of doped Poly1 layer 2810 (not shown in FIGURE 31).

5 Similarly, the etch procedure also etches through the Inter Poly Dielectric (IPD) layer 3000 and the undoped Poly1 layer 2700 down to the P+ sinker 920 in the PNP device.

[00121] In the next step of the manufacturing method of the invention a mask and etch procedure is performed to etch portions
10 of the Inter Poly Dielectric (IPD) layer 3000 and portions of the Poly1 layer 2700 and protective poly layer 2510 over the NMOS device and over the PMOS device. FIGURE 32 illustrates the mask and etch procedure. A photoresist mask 3200 is placed over the four semiconductor devices. Openings are etched through the
15 photoresist mask 3200 over the NMOS device and over the PMOS device. The photoresist mask 3200 covers the NPN device and the PNP device.

[00122] As shown in FIGURE 32, the etch procedure etches through the Inter Poly Dielectric (IPD) layer 3000 and the Poly1
20 layer 2700 and the polysilicon layer 2510 located on each side of the doped Poly1 layer 2820 to form an NMOS gate 2820 in the NMOS device. The etch procedure also etches through portions of the doped Poly1 layer 2820 and protective poly layer 2510 to decrease the length of the doped Poly1 layer 2820. The etch procedure also
25 etches through the Inter Poly Dielectric (IPD) layer 3000 and the

Poly1 layer 2700 and the polysilicon layer 2510 down to the P+ well contact 930 in the NMOS device.

[00123] As also shown in FIGURE 32, the etch procedure etches through the Inter Poly Dielectric (IPD) layer 3000 and the Poly1 layer 2700 and the polysilicon layer 2510 located on each side of the doped Poly1 layer 2920 to form a PMOS gate 2920 in the PMOS device. The etch procedure also etches through portions of the doped Poly1 layer 2920 to decrease the length of the doped Poly1 layer 2920. The etch procedure also etches through the Inter Poly Dielectric (IPD) layer 3000 and the Poly1 layer 2700 and the polysilicon layer 2510 down to the N+ well contact 830 in the PMOS device.

[00124] In this advantageous embodiment of the invention the Poly1 layer 2700 and the Inter Poly Dielectric (IPD) layer 3000 for the MOS devices are masked and etched in two separate steps due to the numerous and sometimes conflicting requirements for the etches. Persons who are skilled in the art will recognize that these mask and etch steps could be combined into one step.

[00125] In the next step of the manufacturing method of the invention the photoresist mask 3200 is removed and a rapid thermal processing (RTP) and furnace procedure is performed. Diffusion and oxidation causes dopant from the extrinsic bases to diffuse into the diffused extrinsic base areas of the NPN device and the PNP device. FIGURE 33 illustrates the result of this procedure. In the NPN device dopant from the doped Poly1 layer

3120 (extrinsic base 3120) diffuses into the diffused extrinsic base area 3310 and dopant from the doped Poly1 layer 3130 (extrinsic base 3130) diffuses into the diffused extrinsic base area 3320. In the PNP device dopant from the doped Poly1 layer 5 3140 (extrinsic base 3140) diffuses into the diffused extrinsic base area 3330 and dopant from the doped Poly1 layer 3150 (extrinsic base 3150) diffuses into the diffused extrinsic base area 3340. In an advantageous embodiment of the invention the depth of each of the doped diffused extrinsic base areas 3310, 10 3320, 3330 and 3340, is approximately one thousand five hundred Ångstroms (1500 Å) or fifteen hundredths of a micron (0.15 μ).

[00126] At the same time, a screen oxide layer 3350 is grown over the intrinsic base areas and the sinkers of the NPN device and the PNP device. The thickness of the screen oxide layer 3350 15 is approximately one hundred fifty Ångstroms (150 Å) or fifteen thousandths of a micron (0.015 μ). Screen oxide layer 3350 is shown in FIGURE 33. For clarity screen oxide layer 3350 will not be shown in the remaining drawings.

[00127] Persons who are skilled in the art will recognize that 20 based on the constraints of the intrinsic base implants and the spacer deposition and etchback, it is possible to skip this heat cycle and combine this heat cycle into one or more other heat cycles.

[00128] In the next step of the manufacturing method of the 25 invention an implantation procedure is used to dope an intrinsic

base of the NPN device and to dope Lightly Doped Drains (LDDs) in the PMOS device. The procedure is illustrated in FIGURE 34. A photoresist mask 3400 is placed over the four semiconductor devices. Openings are etched through the photoresist mask 3400
5 over the NPN device and over the PMOS device. The photoresist mask 3400 covers the PNP device and the NMOS device.

[00129] The four arrows in FIGURE 34 illustrate the implant doping procedure for doping the intrinsic base 3410 in the NPN device. The two arrows in FIGURE 34 illustrate the implant doping
10 procedure for doping the Lightly Doped Drains (LDDs) in the PMOS device. The two Lightly Doped Drains (LDDs) in the PMOS device are denoted with reference numerals 3420 and 3430.

[00130] In this advantageous embodiment of the invention the implant is conducted at a large angle and at four rotations of
15 the semiconductor wafer.

[00131] In the next step of the manufacturing method of the invention an implantation procedure is used to dope an intrinsic base of the PNP device and to dope Lightly Doped Drains (LDDs) of the NMOS device. The procedure is illustrated in FIGURE 35.
20 A photoresist mask 3500 is placed over the four semiconductor devices. Openings are etched through the photoresist mask 3500 over the PNP device and over the NMOS device. The photoresist mask 3500 covers the NPN device and the PMOS device.

[00132] The four arrows in FIGURE 35 illustrate the implant
25 doping procedure for doping the intrinsic base 3510 in the PNP

device. The two arrows in FIGURE 35 illustrate the implant doping procedure for doping Lightly Doped Drains (LDDs) in the NMOS device. The two Lightly Doped Drains (LDDs) in the NMOS device are denoted with reference numerals 3520 and 3530.

5 [00133] In this advantageous embodiment of the invention the implant is conducted at a large angle and at four rotations of the semiconductor wafer.

[00134] In the next step of the manufacturing method of the invention a nitride spacer layer is deposited over the four
10 semiconductor devices. FIGURE 36 illustrates the location of the nitride spacer layer 3600. In an advantageous embodiment of the invention the thickness of each of the nitride spacer layer 3600 is approximately two thousand nine hundred Ångstroms (2900 Å) or twenty nine hundredths of a micron (0.290 μ). Persons who are
15 skilled in the art will recognize that other materials could be used in place of the nitride spacer layer 3600.

[00135] In the next step of the manufacturing method of the invention the nitride spacer layer 3600 is etched back as shown in FIGURE 37. The portions of nitride spacer layer 3600 that
20 remain after the etching procedure form protective sidewalls for the elements of the four semiconductor devices.

[00136] In the next step of the manufacturing method of the invention portions of the screen oxide layer 3350 that are not covered by the nitride spacer layer 3600 are removed from the
25 intrinsic base areas of the NPN device and the PNP device and

from the source drain areas of the NMOS device and the PMOS device and a layer of polysilicon (Poly2) is deposited over the four semiconductor devices. FIGURE 38 illustrates the location of the polysilicon (Poly2) layer 3800. In an advantageous embodiment of the invention the thickness of the polysilicon (Poly2) layer 3800 is approximately two thousand Angstroms (2000 Å) or twenty hundredths of a micron (0.20 μ). Persons who are skilled in the art will recognize that a thin oxide layer will be formed between the Poly2 layer 3800 and the monocrystalline silicon. In an advantageous embodiment of the invention the thickness of this interfacial oxide layer is approximately twelve Angstroms (12 Å) to fifteen Angstroms (15 Å) or approximately twelve ten thousandths of a micron (0.0012 μ) to fifteen ten thousandths of a micron (0.0015 μ).

[00137] In an advantageous embodiment of the invention a thermal process is now performed to break up the interfacial oxide layer between the Poly2 layer 3800 and the intrinsic base in the monocrystalline silicon area. At the same time, damage from the implant of the intrinsic bases is annealed and the intrinsic bases are driven in a heat step that is independent from the step used to drive the emitter dopant. Persons who are skilled in the art will recognize that this step may be combined with the emitter drive heat cycle.

[00138] In the next step of the manufacturing method of the invention a portion of the Poly2 layer (polysilicon layer 3800)

is doped in the NPN device and in the NMOS device and in the PMOS device. FIGURE 39 illustrates the implantation procedure. A photoresist mask 3900 is placed over the four semiconductor devices and openings are etched through the photoresist mask 3900
5 over the NPN device and over the NMOS device and over the PMOS device. The five arrows in FIGURE 39 over the NPN device illustrate the implant doping procedure for doping the polysilicon layer 3800 in the NPN device. The doped portion of the emitter of the NPN device is denoted with the reference
10 numeral 3910 (NPN emitter 3910). The doped portion of polysilicon layer 3800 over N+ sinker 820 is denoted with the reference numeral 3920 (NPN deep collector 3920).

[00139] The four arrows in FIGURE 39 over the NMOS device illustrate the implant doping procedure for doping the
15 polysilicon layer 3800 in the NMOS device. The doped portion of polysilicon layer 3800 in the NMOS device is denoted with the reference numeral 3930 (NMOS source/drain 3930).

[00140] The two arrows in FIGURE 39 over the PMOS device illustrate the implant doping procedure for doping the
20 polysilicon layer 3800 in the PMOS device. The doped portion of polysilicon layer 3800 in the PMOS device is denoted with the reference numeral 3940 (PMOS well contact 3940).

[00141] In the next step of the manufacturing method of the invention a portion of the Poly2 layer (polysilicon layer 3800)
25 is doped in the PNP device and in the NMOS device and in the PMOS

device. FIGURE 40 illustrates the implantation procedure. A photoresist mask 4000 is placed over the four semiconductor devices and openings are etched through the photoresist mask 4000 over the PNP device and over the NMOS device and over the PMOS device. The five arrows in FIGURE 40 over the PNP device illustrate the implant doping procedure for doping the polysilicon layer 3800 in the PNP device. The doped portion of the emitter of the PNP device is denoted with the reference numeral 4010 (PNP emitter 4010). The doped portion of polysilicon layer 3800 over P+ sinker 920 is denoted with the reference numeral 4020 (PNP deep collector 4020).

[00142] The two arrows in FIGURE 40 over the NMOS device illustrate the implant doping procedure for doping the polysilicon layer 3800 in the NMOS device. The doped portion of polysilicon layer 3800 in the NMOS device is denoted with the reference numeral 4030 (NMOS well contact 4030).

[00143] The four arrows in FIGURE 40 over the PMOS device illustrate the implant doping procedure for doping the polysilicon layer 3800 in the PMOS device. The doped portion of polysilicon layer 3800 in the PMOS device is denoted with the reference numeral 4040 (PMOS source/drain 4040).

[00144] In the next step of the manufacturing method of the invention portions of the Poly2 layer (polysilicon layer 3800) are etched to define the emitters and collectors of the NPN device and of the PNP device and to define the sources and drains

of the NMOS device and of the PMOS device. As shown in FIGURE 41, the photoresist mask 4000 from the previous step is removed and a photoresist mask 4100 is placed over the four semiconductor devices.

5 [00145] The etch procedure etches away exposed portions of the Poly2 layer 3800 and exposed portions of the sidewalls formed from nitride layer 3600. The etch procedure also etches away end portions of the doped Poly2 layer 3910 (NPN emitter 3910) and end portions of the doped Poly2 layer 3920 (NPN deep collector 3920)
10 in the NPN device. The etch procedure also etches away end portions of the doped Poly2 layer 4010 (PNP emitter 4010) and end portions of the doped Poly2 layer 4020 (PNP deep collector 4020) in the PNP device.

[00146] The etch procedure also etches through a central
15 portion of the doped Poly2 layer 3930 (NMOS source/drain 3930) in the NMOS device down to the Inter Poly Dielectric (IPD) layer 3000. This separates the source portion from the drain portion in the NMOS device. The etch procedure also etches away end portions of the doped Poly2 layer 4030 (NMOS well contact 4030) in the
20 NMOS device.

[00147] The etch procedure also etches through a central portion of the doped Poly2 layer 4040 (PMOS source/drain 4040) in the PMOS device down to the Inter Poly Dielectric (IPD) layer 3000. This separates the source portion from the drain portion in
25 the PMOS device. The etch procedure also etches away end portions

of the doped Poly2 layer 3940 (PMOS well contact 3940) in the PMOS device.

[00148] In the next step of the manufacturing method of the invention an etch procedure is performed to etch portions of the
5 Inter Poly Dielectric (IPD) layer 3000 and portions of the trench fill material on each of the four semiconductor devices. As shown in FIGURE 42 the exposed portions of the Inter Poly Dielectric (IPD) layer 3000 are removed. The central portion of the Inter Poly Dielectric (IPD) layer 3000 over the doped polysilicon
10 (Poly1) layer 2820 (NMOS gate 2820) in the NMOS device is etched away. The central portion of the Inter Poly Dielectric (IPD) layer 3000 over the doped polysilicon (Poly1) layer 2920 (PMOS gate 2920) in the PMOS device is also etched away. In addition, portions of the trench fill material 1710 on each of the four
15 semiconductor devices are etched away as shown in FIGURE 42.

[00149] In the next step of the manufacturing method of the invention the photoresist mask 4100 is removed and a rapid thermal processing (RTP) procedure is performed to activate the PNP emitter, the NPN emitter, the source and drain of the NMOS
20 device, and the source and drain of the PMOS device. FIGURE 43 illustrates the result of applying the RTP procedure. Diffusion and oxidation causes dopant from the NPN emitter 3910 to diffuse into the intrinsic base 3410 of the NPN device. The doped area is denoted with the reference numeral 4310 (emitter region 4310).

[00150] Similarly, diffusion and oxidation causes dopant from the PNP emitter 4010 to diffuse into the intrinsic base 3510 of the PNP device. The doped area is denoted with the reference numeral 4320 (emitter region 4320).

5 [00151] In addition, diffusion and oxidation causes dopant from the doped polysilicon (Poly2) layer 3930 in the NMOS device to diffuse into the Lightly Doped Drain (LDD) 3520 and into the Lightly Doped Drain (LDD) 3530 in the NMOS device. The area doped in LDD 3520 is denoted with the reference numeral 4330. The area
10 doped in LDD 3530 is denoted with the reference numeral 4340.

[00152] Similarly, diffusion and oxidation causes dopant from the doped polysilicon (Poly2) layer 4040 in the PMOS device to diffuse into the Lightly Doped Drain (LDD) 3420 and into the Lightly Doped Drain (LDD) 3430 in the PMOS device. The area doped
15 in LDD 3420 is denoted with the reference numeral 4350. The area doped in LDD 3430 is denoted with the reference numeral 4360. The results of these steps are illustrated in FIGURE 43.

[00153] FIGURE 44 illustrates a diagrammatic plan view of the top of an exemplary rectangular opening etched into the doped
20 Poly1 layer 2910 of the NPN semiconductor device. The outer portions 4400 around the opening represent the surrounding shallow trench with oxide fill. The portions denoted with reference numeral 4410 represent the doped layer of Poly1 material 2910 (and overlying Inter Poly Dielectric (IPD) layer
25 3000). The dotted line 4420 denotes the extent of the area of

monocrystalline silicon under the Poly1 material 2910 (and the overlying IPD layer 3000). The inner rectangle denoted with reference numeral 4430 represents the spacer material 3600. The portion denoted with reference numeral 4440 represents the area of the intrinsic base 3410 in the monocrystalline silicon portion
5 of the NPN device.

[00154] The intrinsic base implant 3410 goes into the monocrystalline silicon area 4440 in the center of the rectangle. The spacer material 3600 forms an inner rectangle 4430 inside the
10 center of the Poly1/IPD rectangle 4410. When the doped Poly2 layer 3910 is placed in contact with the monocrystalline silicon area 4440, then the spacer material 3600 separates the doped Poly2 layer 3910 from all four inner walls of the Poly1/IPD material. A similar structure is also used in the PNP
15 semiconductor device.

[00155] In the next step of the manufacturing method of the invention a cobalt silicide layer is formed over the four semiconductor devices. FIGURE 45 illustrates the location of the cobalt silicide layer 4500. The cobalt silicide layer 4500 covers
20 all polysilicon Poly2 layers and all polysilicon Poly1 layers that are not under a polysilicon Poly2 layer. In an advantageous embodiment of the invention the thickness of each of the cobalt silicide layer 4500 is approximately two hundred fifty Ångstroms (250 Å) or twenty five thousandths of a micron (0.025 μ).

[00156] Persons who are skilled in the art will recognize that alternative silicides could also be used (e.g., titanium). Alternatively, the device could be made without silicide.

[00157] In the next step of the manufacturing method of the invention a layer of tetra ethyl ortho silicate (TEOS) is deposited over the four semiconductor devices. FIGURE 46 illustrates the location of the TEOS layer 4600. In an advantageous embodiment of the invention the thickness of the TEOS layer 4600 is approximately six thousand five hundred
10 Ångstroms (6500 Å) or sixty five hundredths of a micron (0.65 μ).

[00158] In the next step of the manufacturing method of the invention a mask and etch procedure is performed to etch portions of the TEOS layer 4600 over the four semiconductor devices to receive metal contacts. A contact photoresist mask (not shown)
15 is placed over the four semiconductor devices. An etch procedure then etches the TEOS layer 4600 down to the level of the cobalt silicide 4500. The result is shown in FIGURE 47. Contact receptacle 4710 and contact receptacle 4720 are formed in the TEOS layer 4600 of the NPN device. Contact receptacle 4730 and
20 contact receptacle 4740 are formed in the TEOS layer 4600 of the PNP device.

[00159] Similarly, contact receptacle 4750, contact receptacle 4760 and contact receptacle 4770 are formed in the TEOS layer 4600 of the NMOS device. Contact receptacle 4780, contact

receptacle 4790 and contact receptacle 4795 are formed in the TEOS layer 4600 of the NMOS device.

[00160] In the next step of the manufacturing method of the invention metal contacts are placed within the contact
5 receptacles in the four semiconductor devices. The result is shown in FIGURE 48. Metal contact 4810 is placed within contact receptacle 4710 and metal contact 4820 is placed within contact receptacle 4720 in the NPN device. Metal contact 4830 is placed within contact receptacle 4730 and metal contact 4840 is placed
10 within contact receptacle 4740 in the PNP device.

[00161] Metal contact 4850 is placed within contact receptacle 4750 and metal contact 4860 is placed within contact receptacle 4760 and metal contact 4870 is placed within contact receptacle 4770 in the NMOS device.

15 [00162] Metal contact 4880 is placed within contact receptacle 4780 and metal contact 4890 is placed within contact receptacle 4790 and metal contact 4895 is placed within contact receptacle 4795 in the NMOS device.

[00163] FIGURE 49 illustrates a diagrammatic top plan view of
20 the layout of an exemplary bipolar transistor (NPN or PNP) of the invention. The outer portions 4900 represent the surrounding shallow trench with oxide fill. The portions denoted with reference numeral 4910 represent the doped layer of Poly1 material. The dotted line 4920 denotes the extent of the area of
25 monocrystalline silicon under the Poly1 material. The dotted

line 4930 denotes the location of the opening through the Poly1 / IPD layer down to the underlying monocrystalline silicon area (including the spacer material). The rectangle 4940 denotes the location of the doped Poly2 layer. In the area under Poly2 and over Poly1, the IPD remains between the two poly layers. Rectangle 4950, rectangle 4960 and rectangle 4970 each represent a contact hole in the TEOS filled with metal. Those persons who are familiar with the art will recognize that the emitter contact 4950 has been offset from the emitter hole in this advantageous embodiment of the invention. This permits the emitter area and surrounding monocrystalline extrinsic base area to be smaller which offers certain performance advantages. In the event that the performance advantages are not necessary, the emitter contact 4950 could be placed directly over the emitter doped Poly2 in contact with the monocrystalline intrinsic base 4930.

[00164] FIGURE 50 illustrates a diagrammatic top plan view of the layout of an exemplary metal oxide semiconductor (MOS) transistor (NMOS or PMOS) of the invention. The outer portions 5000 represent the surrounding shallow trench with oxide fill. The portion denoted with reference numeral 5010 represents the Poly2 layer doped with emitter (the MOS source / drain). The dotted line 5020 denotes the extent of the area of active monocrystalline silicon under the Poly1 material. The portion denoted with reference numeral 5030 represents the area of the Poly1 material that is doped with extrinsic base (the MOS gate).

The dotted line 5040 represents the location of the Poly1 / IPD layer underlying the overlap of the Poly2 material. Rectangle 5050, rectangle 5060 and rectangle 5070 each represent a contact hole in the TEOS filled with metal.

5 [00165] Those persons who are familiar with the art will recognize that the gate contact 5050 has been offset from the part of the gate poly enclosed by Poly2 in this advantageous embodiment of the invention. This permits the gate length to be smaller which offers certain performance advantages. In the event
10 that these performance advantages are not necessary, the gate contact 5050 could be placed directly on the gate poly between the source Poly2 and drain Poly2.

[00166] An advantageous embodiment of the invention has been described in which two types of double poly bipolar transistors
15 (NPN and PNP) are present in combination with two types of double poly MOS transistors (NMOS and PMOS). Persons who are skilled in the art will understand that alternate embodiments of the invention may comprise a combination of any two of the types of double poly transistors.

20 [00167] A combination of a PMOS transistor and an NPN bipolar transistor may be made by adding one mask for a P source drain. A combination of an NMOS transistor and a PNP bipolar transistor may be made by adding one mask for an N source drain. A combination of an NMOS transistor and an NPN bipolar transistor
25 may be made by adding two masks for an NMOS Lightly Doped Drain

(LDD) and an NMOS gate. A combination of a PMOS transistor and a PNP bipolar transistor may be made by adding two masks for a PMOS Lightly Doped Drain (LDD) and a PMOS gate.

[00168] Although the present invention has been described with
5 an exemplary embodiment, various changes and modifications may be suggested to one skilled in the art. It is intended that the present invention encompass such changes and modifications as fall within the scope of the appended claims.